What is claimed is:

1. A quadrature modulation transmitter comprising:

a digital processing block for receiving an I-channel data, a Q-channel data and a clock signal, modulating the I-channel data or an inverted I-channel data into a first analog signal by means of an I-channel DAC according to a switching of an I-clock signal identical to the clock signal, and modulating the Q-channel data and an inverted Q-channel data into a second analog signal by means of a Q-channel DAC according to a switching of a Q-clock signal, the Q-clock signal being an inverted clock signal; and

an analog processing block for receiving the first and second analog signals from the digital processing block, adding the first and second analog signals, converting the added signal into an RF domain signal through a mixing operation, and amplifying and transmitting the RF domain signal.

2. The quadrature modulation transmitter as recited in claim 1, wherein the digital processing block includes:

a first inverter for inverting the I-channel data;

a first T flip-flop for receiving the I-clock signal through a clock terminal and outputting a first switch control signal according to the I-clock signal;

a first switch for turning on an output of the first inverter in case a output of the first T flip-flop is in a

first logic level and for turning on the I-channel data in case the output of the first T flip-flop is in a second logic level;

a first DAC for receiving the I-clock signal through a clock terminal, converting an output of the first switch into an analog signal and simultaneously performing a modulation;

a second inverter for inverting the clock signal and outputting the resulting value as the Q-clock signal;

a third inverter for inverting the Q-channel data;

a second T flip-flop for receiving the Q-clock signal through a clock terminal and outputting a second switch control signal according to the Q-clock signal;

a second switch for turning on an output of the third inverter in case an output of the second T flip-flop is in a first logic level and for turning on the Q-channel data in case the output of the second T flip-flop is in a second logic level; and

a second DAC for receiving the Q-clock signal through a clock terminal, converting an output of the second switch into an analog signal and simultaneously performing a modulation.

3. The quadrature modulation transmitter as recited in claim 1, further comprising a digital filter for matching a conversion speed of I-channel and Q-channel digital data outputted from a modem with an intermediate frequency and outputting the resulting data as the I-channel and Q-channel data to the digital processing block.